WE CLAIM

1. A processor operable to perform a plurality of functions, said processor comprising:

an input port;

a storage element operable to receive and to store an input signal input via said input port, said input signal comprising at least one control value;

control logic operable to control at least one of said functions of said processor in dependence on said at least one control value; and

access logic operable to receive an access control signal and to disable access via said input port to said at least one control value stored in said storage element in dependence upon said access control signal.

2. A processor according to claim 1, wherein access disabled via said input port is write access.

3. A processor according to claim 1, wherein said access control signal is non-reversibly set to a value such that access via said input port is permanently disabled.

4. A processor according to claim 1, said processor being operable in a plurality of modes and a plurality of domains said plurality of domains comprising a first domain and a second domain, and said processor further comprising:

monitoring logic operable to perform a diagnostic function and capture diagnostic data from said processor; wherein

said control value is indicative of whether said diagnostic function is available to capture diagnostic data from said first domain; and

said control logic is operable to control availability of said diagnostic function in dependence on said at least one control value stored in said storage element.

5. A processor according to claim 4, wherein said first domain is a secure domain and said second domain is a non-secure domain, said processor being operable

such that when executing a program in a secure mode within said secure domain said program has access to secure data which is not accessible when said processor is operating in a non-secure mode in said non-secure domain.

6. A processor according to claim 4, wherein said monitoring logic comprises logic operable to perform a debug function.

7. A processor according to claim 4, wherein said monitoring logic comprises logic operable to perform a trace function.

8. A processor according to claim 4, wherein said control value relates to a condition and is indicative of whether said monitoring logic is available to capture diagnostic data from said first domain when said condition is present.

9. A processor according to claim 8, wherein said condition comprises monitoring type, domain, mode.

10. A processor according to claim 4, wherein said storage element is operable to receive and store a signal from said processor operating in said first domain, said signal comprising at least one control value.

11. A processor according to claim 5, wherein said input port comprises an input port on a JTAG controller.

12. A processor according to claim 11, said access logic comprising a gate, said gate being arranged to receive said access control signal and said signal input via said input port, said gate being operable to output no signal to said storage element when said access control signal is set to a predetermined level.

13. A processor according to claim 12, wherein said access control signal is permanently tied to said predetermined level.

14. A method of controlling a processor operable to perform a plurality of functions, said method comprising said steps of:

setting at least one control value via an input port to said processor, said at least one control value relating to at least one of said functions of said processor, said operation of said at least one function being controlled in dependence upon said control value; and

disabling access to said at least one control value via said input port in dependence upon an access control signal.

15. A method according to claim 14, wherein said step of disabling access comprises disabling write access.

16. A method according to claim 14, wherein said step of disabling access comprises non-reversibly setting said access control signal to a value such that access via said input port is permanently disabled.

17. A method according to claim 14, wherein said processor is operable to control an availability of a diagnostic function operable to capture diagnostic data from said processor, said processor being operable in a plurality of modes and a plurality of domains, said plurality of domains, comprising a first domain and a second domain; and

said at least one control value is indicative of whether said diagnostic function is available to capture diagnostic data from said first domain

18. A method according to claim 17, wherein said first domain comprises a secure domain and said second domain comprises a non-secure domain, said processor being operable such that when executing a program in a secure mode within said secure domain said program has access to secure data which is not accessible when said processor is operating in a non-secure mode within said non-secure domain.

19. A method according to claim 17, wherein said diagnostic function comprises a debug function.

20. A method according to claim 17, wherein said diagnostic function comprises a trace function.

21. A method according to claim 17, wherein said control value relates to a condition and is indicative of whether said monitoring logic is available to capture diagnostic data from said first domain when said condition is present.

22. A method according to claim 21, wherein said condition comprises domain, type of monitoring function, mode.

23. A method according to claim 14, wherein said input port comprises an input port on a JTAG controller